

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

VLSI TECHNOLOGY LLC,
Plaintiff,

v.

INTEL CORPORATION,
Defendant.

Case No. 1:19-cv-977-ADA

**DECLARATION OF PROFESSOR THOMAS M. CONTE
IN SUPPORT OF
PLAINTIFF VLSI TECHNOLOGY LLC'S
OPENING CLAIM CONSTRUCTION BRIEF**

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DECLARATION OF THOMAS M. CONTE

I, **Thomas M. Conte**, declare as follows:

1. I have been asked to provide technological background regarding the patents involved in this case and some of the claim terms they contain. I have personal knowledge of the facts stated in this declaration and, if called as a witness, would affirm the truthfulness of each statement herein.

I. BACKGROUND AND QUALIFICATIONS

2. I am a Professor of Computer Science and of Electrical & Computer Engineering at Georgia Institute of Technology ("Georgia Tech"), a position that I've held since mid-2008. Prior to that, I was a Professor of Electrical & Computer Engineering at North Carolina State University ("NC State"), from July 1995 to June 2008. I was an assistant professor of Electrical & Computer Engineering at the University of South Carolina from 1992 to 1995.

3. I received my Bachelor of Electrical Engineering degree from the University of Delaware in 1986; I received my Master of Science in Electrical Engineering from the University of Illinois at Urbana-Champaign in 1988; and I received my Doctor of Philosophy in Electrical Engineering from the University of Illinois at Urbana-Champaign in 1992.

4. I am a Fellow of the Institute of Electrical and Electronic Engineers ("IEEE"). I am the past chair of the IEEE Computer Society's Technical Committee on Microarchitecture and Microprogramming, and past Chair of the ACM Special Interest Group on Microarchitecture. I am a past Editor in Chief of the ACM Transactions on Architecture and Compiler Optimization. I am or have been an Associate Editor of several journals, including the Journal on Instruction Level Parallelism, IEEE Embedded Systems Letters, the IEEE Micro magazine, the IEEE Computer magazine, IEEE Transactions on Computers, and ACM Transactions on Embedded Computer Systems.

5. I served as the President of the IEEE Computer Society in 2015. Since 2016, I have served as the vice chair of the International Roadmap for Devices and Systems.

6. I served as the Chief Microarchitect and Manager of the Back-End Compiler team for digital signal microprocessor maker BOPS, Inc.

7. I am an author of over 90 peer-reviewed technical publications in the field of computer engineering, electrical engineering, or computer science, many of which are frequently cited and several of which have won Best Paper awards. I am a named inventor on 40 issued U.S. Patents.

8. I have attached my curriculum vitae as Exhibit A to this Declaration. It includes the above-listed credentials and additional information on my background and experience, as well as list of cases in which I have served as an expert witness within the past four years.

II. DISCUSSION

9. The discussion below is provided after a careful review of the relevant patents and other intrinsic evidence, including the file histories and cited prior art.

A. The Person Having Ordinary Skill In The Art

10. It is my opinion that a person having ordinary skill in the art in the context of the patents would hold a Bachelor's Degree in electrical engineering, computer engineering or a related field, and have approximately three years of relevant industry experience (or equivalent experience).

B. U.S. Patent No. 7,292,485 (The '485 Patent)

11. The '485 Patent is titled "SRAM Having Variable Power Supply And Method Therefor." It relates to improving the stability and write margins of SRAM memory cells. *See, e.g., Ex. 2,*¹ Abstract.

1. "capacitance structure" (claims 1-6, 8-14, 16-20)

12. Several independent and dependent claims of the '485 Patent refer to a "capacitance structure." These claims refer both to a "first capacitance structure" and a "second capacitance structure." The specific physical structures that may comprise the capacitance structure can vary from claim to claim. For example, claims 1 and 12 recite "a first capacitance structure includes a plurality of dummy cells," while claim 19 recites "the capacitance structure comprises: a dummy line; a plurality of dummy cells adjacent to and coupled to the dummy line; and a first dummy cell adjacent to but not coupled to the dummy line."

13. I understand that Intel has proposed construing "capacitance structure" as a means-plus-function term under Section 112(6). I have been informed that when a claim term lacks the word "means" (as is the case here), there is a presumption that Section 112(f) does not apply. I am further informed that Section 112(f) does not apply if "the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." Applying these principles, a person of skill in the art would not conclude that "capacitance structure" was intended to be interpreted as a means-plus-function term.

¹ All numbered exhibits are attached to the Declaration of Charlotte J. Wen concurrently filed herewith.

**(a) A Person Of Ordinary Skill In The Art Would Understand
"Capacitance Structure" By Its Plain And Ordinary Meaning**

14. A person of skill in the art would understand that the term "capacitance structure" to have its plain and ordinary meaning, which encompasses a well-known class of structures, such as those on a memory circuit, that have capacitance. Such structures can include, for example, transistors, capacitors, dummy cells, and arrangements of the same, which have capacitance.

15. "Capacitance" is not a function. Capacitance is a physical property (like mass, temperature, resistance, or inductance). It refers to the capability of a physical structure, or system, to hold electric charge.

16. The '485 Patent and prosecution history support my conclusion that a "capacitance structure" would be understood by a person of skill in the art as described above. For example, certain structures are described by the '485 Patent as having "capacitance" or "relative capacitances." *See, e.g.*, Ex. 2, 4:5-7 ("Dummy column 17 is used for capacitance sharing with memory array 14 during a write operation. The amount of capacitance shared is determined in part by how many memory cells are coupled to conductor 37."); Ex. 2, 4:43-46 ("Charge sharing occurs between the selected columns of the memory array 14 and the dummy column 17 to reduce the supply voltage of memory array 14 by a predetermined amount depending on the relative capacitances of dummy column 17 and the selected columns of memory array 14."); Ex. 2, 4:47 ("The capacitance of dummy column 17 can be adjusted"); *see also, e.g.*, Ex. 2, 4:64-66; Ex. 2 at 6:27-30.

(b) The '485 Patent Repeatedly Describes "Capacitance Structure" In Terms Of Its Physical Interactions With Other Structures On The Claimed Memory Circuit

17. I understand courts regularly find that if a patent repeatedly describes a claim term in terms of its interactions with other physical structures, then the claim term recites sufficiently definite structure to avoid application of Section 112, ¶ 6.

18. The claims, the specification, and the prosecution history repeatedly describe the "capacitance structure" in terms of its physical interactions with other structures on the claimed memory circuits.

19. For instance, many of the '485 Patent claims also impose additional physical requirements for the claimed "capacitance structure." Examples include:

- Claim 1 recites "a first capacitance structure includes a plurality of dummy cells."
- Claim 3 recites "the first capacitance structure comprises: a dummy line; and the plurality of dummy cells coupled to the dummy line."
- Claim 10 recites "the first capacitance structure comprises a first line and a first plurality of dummy cells coupled to the first line" and "the second capacitance structure comprises a second line and a second plurality of dummy cells coupled to the second line."
- Claim 12 recites "a first capacitance structure includes a plurality of dummy cells."
- Claim 19 recites " the capacitance structure comprises: a dummy line; a plurality of dummy cells adjacent to and coupled to the dummy line; and a first dummy cell adjacent to but not coupled to the dummy line."

20. During prosecution of the '485 Patent, the Examiner amended claims 1 and 12 to add "includes a plurality of dummy cells" after the "capacitance structure" limitation in those claims, Ex. 6 at 2, further confirming that a person of skill in the art would understand "capacitance structure" to recite definite structure.

21. Many of the '485 Patent claims also describe how the "capacitance structure" interacts with other physical structures in the claimed circuit. Examples include:

- Claim 1 recites "a switching circuit that has transistors that . . . couple the second power supply line to the first capacitance structure."
- Claim 6 recites "the switching circuit further comprises a switching transistor coupled between the capacitance structure and a voltage reference terminal."
- Claim 9 recites "the switching circuit further comprising transistors that . . . couple the fourth power supply line to the second capacitance structure."
- Claim 12 recites "a switching circuit that has transistors that connected between the first power supply terminal, the first power supply line, the second power supply line and the first capacitance structure" and "coupling charge from the second power supply line to the first capacitance structure."
- Claim 17 recites "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells."

2. "precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells"

22. Claims 17-19 of the '485 Patent recite a "precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells." I understand that the parties agree that this claim term should be interpreted as a means-plus-function term, and that while the parties agree on the corresponding function ("precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells"), they disagree as to the corresponding structure.

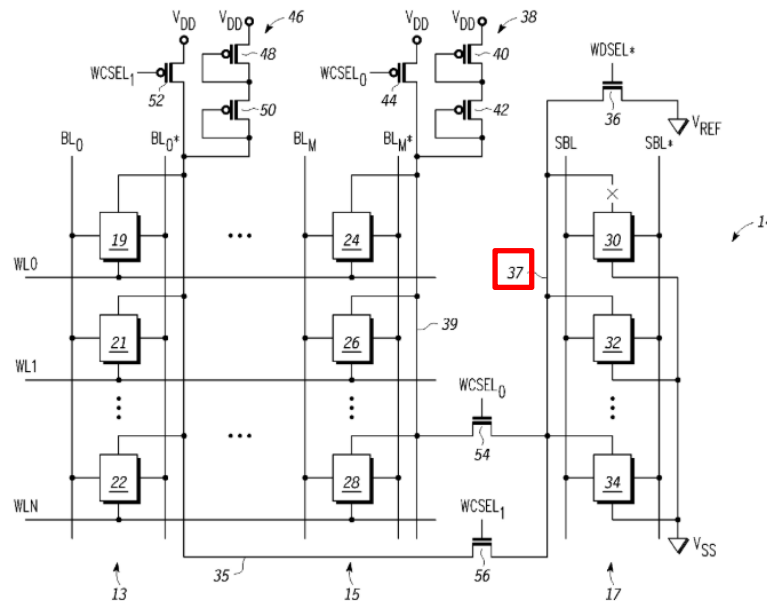
23. I further understand that VLSI has proposed that the structure is "a conductor, or equivalents thereof," and that Intel has proposed that the structure is "(1) Voltage source V_{REF} and transistor 36, coupled in series to provide a reference voltage to one or more dummy cells through conductor 37, as shown in Figure 2; or alternatively (2) voltage source V_{REF} and transistor 90, coupled in series to provide a reference voltage to one or more dummy cells through conductor 71, as shown in Figure 3."

24. I understand that a corresponding structure for a function set forth in a means-plus-function limitation must actually perform the recited function, not merely enable the structure to operate as intended.

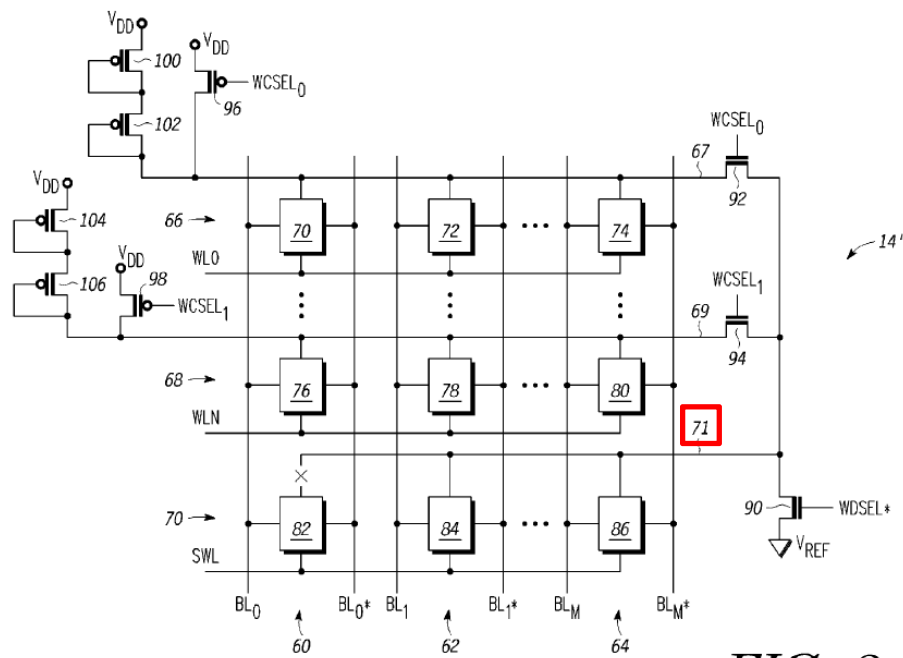
(a) A Person Of Skill In The Art Would Understand That VLSI's Proposed Structure Of "A Conductor, Or Equivalents Thereof" Performs The "Precharging" Function

25. A person of skill in the art would understand, based on the disclosure of the '485 Patent, that a "conductor" is the only structure required to actually perform the "precharging" function. The patent states, for example, that: "In operation, prior to writing . . . [r]eference voltage V_{REF} is provided to the supply terminals of each of the memory cells 30, 32, and 34

precharging the cells of dummy column 17 to V_{REF} (ground)." A person of skill in the art would understand that the cells of dummy column 17 correspond to the recited capacitance structure in this embodiment. Figure 2 illustrates that conductor 37 (label highlighted with a red box) is the structure that precharges (*e.g.*, carries voltage to) the capacitance structure:



26. As another example, the patent states that: "Also prior to a write operation, ... V_{REF} is provided to the supply terminals of each of the memory cells, such as cells 82, 84, and 86, precharging the cells of dummy row 70 to V_{REF} ." Ex. 2, 6:12-16. A person of skill in the art would understand that the cells of dummy row 70 correspond to the recited capacitance structure in this embodiment. Figure 3 illustrates that conductor 71 (label highlighted with a red box) is the structure that precharges the capacitance structure by carrying voltage to it:

**FIG. 3**

27. As still another example, the patent states that "[t]he amount of capacitance shared is determined in part by how many memory cells are coupled to conductor 37." Thus, a person of skill in the art would understand that a conductor is the only structure necessary to perform the function of "precharging" the capacitance structure, as distinguished from other elements that may enable the conductor to operate in that manner.

(b) Intel's Proposed Structure Is Inconsistent With The Disclosure Of The '485 Patent

28. A person of skill in the art would not understand that "(1) Voltage source V_{REF} and transistor 36, coupled in series to provide a reference voltage to one or more dummy cells through conductor 37, as shown in Figure 2; or alternatively (2) voltage source V_{REF} and transistor 90, coupled in series to provide a reference voltage to one or more dummy cells through conductor 71, as shown in Figure 3."

29. As depicted in Figures 2 and 3, it is the conductor that actually precharges the capacitance structure, not "a voltage source V_{REF} and a transistor coupled in series." First, the '485

Patent does not discuss a "voltage source." Second, while the '485 Patent does discuss reference voltages, a person of skill in the art would understand that a reference voltage is not a structure. Indeed, a person of skill in the art would understand that the provision of a "reference voltage" through a transistor merely enables the conductor to carry the voltage to the capacitance structure, *i.e.*, perform the "precharging" function.

30. Similarly, a person of skill in the art would not understand the corresponding structure for the "precharging" function to include "dummy cells." As explained earlier, the "dummy cells" correspond to the "capacitance structure" in some embodiments of the '485 Patent. The dummy cells are therefore the *subject* of the "precharging" function, *i.e.*, the device that is itself precharged, not the structure that performs the precharging function.

31. Thus, the corresponding structure for the function of "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" is "a conductor, or equivalents thereof."

3. "first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" / "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells"

32. Claim 17, and the claims that depend from it, recite a "first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" and a "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells."

33. I understand that the parties agree that this claim term should be interpreted as a means-plus-function term, and that while the parties agree on the functions set forth in the claims,

they disagree as to the corresponding structure. I understand that VLSI has proposed that the structure corresponding to both the first and second "coupling" functions is "a switching circuit, or equivalents thereof."

34. I understand Intel argues that the structure that performs the first "coupling" function is "(1) Transistor 52 and clamping circuit 46, configured to couple power supply voltage VDD and conductor 35, as shown in Figure 2 (if the second line of memory cells is SRAM column 15); or alternatively (2) transistor 96 and a clamping circuit, configured to couple power supply voltage VDD and conductor 67, as shown in Figure 3 (if the second line of memory cells is SRAM row 68)."

35. A person of skill in the art would understand that neither of Intel's proposed transistors (reference numbers 52 and 96) perform the first "coupling" function, which occurs "during the write operation for the second line of memory cells." This is because the patent explicitly states that "During a write operation, one or both of decoded control signals WCSEL₀ and WCSEL₁ are asserted as logic high signals to cause transistors 52 and 44 to be substantially non-conductive," and that "During a write operation, one or both of decoded control signals WCSEL₀ and WCSEL₁ are asserted as logic highs to cause transistors 96 and 98 to be substantially non-conductive." Ex. 2, 4:33-36; *id.*, 6:16-19. When transistors are caused "to be substantially non-conductive," as described here, they are effectively being decoupled. In other words, a person of skill in the art would understand that transistors 52 and 96 are *being decoupled* during the write operation, not performing the first *coupling* function.

36. Similarly, a person of skill in the art would understand that neither of Intel's proposed clamping circuits (including clamping circuit 46) perform the first "coupling function." The patent explicitly explains that, during the write operation, the "clamping circuits function to

limit the voltage drop on conductors 67 and 69," and "clamping circuits 38 and 46 function to limit the voltage drop on conductors 35 and 39." Ex. 2, 6:31-32; *id.*, 4:50-52. A person of skill in the art would therefore understand that the clamping circuits do not perform the first coupling function.

4. "decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells"

37. Claim 17, and the claims that depend from it, recite a "decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells."

38. I understand that the parties agree that this term invokes Section 112(f). I further understand that the parties agree the claimed function is "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells." I also understand that the parties dispute whether the '485 Patent recites structure to perform this "decoupling" function.

39. A person of skill in the art would understand that the '485 Patent clearly discloses a "switching circuit" as performing the function of "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells."

40. For example, the abstract states: "For the case where the second line of memory cells is selected for writing, a switching circuit couples the power supply terminal to the first power supply line, decouples the first power supply line from the second line of memory cells, and couples the second power supply line to the first capacitance structure." Ex. 2, Abstract.

41. As another example, the specification states: "Generally, in one embodiment, a memory circuit comprises a memory array having a first line of memory cells, a second line of memory cells, a first power supply terminal, and a first capacitance structure. A first power supply

line is coupled to the first line of memory cells. A second power supply line is coupled to the second line of memory cells. A switching circuit that has transistors that, when the second line of memory cells is selected for writing, couple the first power supply terminal to the first power supply line, decouple the first power terminal from the second line of memory cells, and couple the second power supply line to the first capacitance structure." Ex. 2, 6:47-58.

42. Thus, a person of skill in the art would understand that the "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" function is performed by a switching circuit, or equivalents thereof.

C. U.S. Patent No. 7,793,025 (The '025 Patent)

43. The '025 Patent is titled "Hardware managed context sensitive interrupt priority level control." The patent describes "[a] flexible interrupt controller circuit and methodology," that can handle external interrupt requests in different ways based on system mode. Ex. 5, Abstract. Examples of system modes include "OS context ID, power management modes, security modes, and other system defined modes where priority levels would differ." *Id.*

1. Interrupt requests

44. The patent states: "In computer systems, an interrupt is an asynchronous signal from hardware indicating the need for attention or a synchronous event in software indicating the need for a change in execution." Ex. 5, 1:14-16.

45. There are a number of different types of interrupt requests. I describe some of them below, together with examples of how they are often understood and their usage in the '025 Patent.

- a. Potential interrupt request: *e.g.*, possible future requests that have not yet been issued, but might be issued at some later point. *See, e.g.*, Ex. 5, claims 17, 20; 2:54-57 ("For example, an interrupt enable register stores masking bits

corresponding to each of the potential interrupt requests, thereby enabling individual bit masking of the interrupt requests."); *id.*, 2:57-61 ("Each potential interrupt request has a corresponding bit location in the interrupt enable register, and each bit in the interrupt enable register is logically combined (e.g., using a logical AND gate) with the corresponding interrupt request.").

- b. Masked interrupt request: *e.g.*, a request that has been received by the processor but will not be acted upon. *See, e.g., id.*, 1:46-50 ("By logically combining (e.g., with a logical AND gate) the individual bits of the interrupt source register and the content of the interrupt enable register, the interrupt requests may be effectively masked and stored in an interrupt pending register."); *id.*, 2:50-54 ("Hardware and/or software interrupt requests that are presently asserted may be selectively masked to generate a plurality of pending interrupt signals that may be stored in an interrupt pending register included in the interrupt controller."); *id.*, 5:11-17 ("in selected embodiments, each interrupt request 202 is provided directly to the AND gate 208 and is only permitted to pass the AND gate 208 if the interrupt request is enabled in the interrupt enable register 206 (which may also be referred to as a mask register) and other enabling circuitry which selectively masks the interrupts to enable or disable potential interrupts in the data processing system.").
- c. Received interrupt request: *e.g.*, a request that has reached the processor. *See, e.g., id.*, 4:54-58 ("When the interrupt source register 204 is implemented as a storage device or a routing circuit, the register 204 receives a plurality of inputs 202 which may correspond to hardware and/or software interrupt requests from

various interrupt sources that are received by the interrupt circuit 200."); *id.*, 4:58-63 ("These interrupt requests may be received via physical conductors, such as the integrated circuit terminals 40, where each of the interrupt requests 202 corresponds to a particular interrupt source."); *id.*, 4:65-5:3 ("The interrupt source register 204 selectively stores all interrupt requests received via the physical conductors or from on-chip sources, or alternatively routes the received interrupt requests to the CPU, thereby providing a monitoring pathway for the CPU to read the interrupt source(s) 202.").

- d. Pending interrupt request: *e.g.*, a request that has been received in the processor but has not yet been acted upon by interrupting program execution. *See, e.g., id.*, 2:61-63 ("Results of the logical combination operation specify one or more enabled, pending interrupt requests, which may be stored in an interrupt pending register."); *id.*, 3:7-12 ("A priority encoder may be used to logically combine the pending interrupt requests with the contents of the interrupt priority register that is selected based on the current context of processor that is to service the interrupt request(s), thereby generating an interrupt request signal that is provided to the processor."); *id.*, 10:2-6 ("The disclosed data processing system includes one or more interrupt sources for generating a pending interrupt requests, including specifically a first interrupt source for generating a pending interrupt request."); *id.*, 10:15-21 ("And a priority encoder is coupled to receive the pending interrupt request and the selected priority level information, and to use the selected priority level information to prioritize the pending interrupt

request, thereby providing a prioritized interrupt request signal which will cause an interrupt to occur in the data processing system.").

- e. Handled interrupt request: *e.g.*, a request that has been received and acted upon by interrupting program execution and executing an interrupt handler. *See, e.g., id.*, 1:16-18 ("A hardware interrupt causes the processor to save its state of execution via a context switch, and begin execution of an interrupt handler."); *see also* U.S. Patent No. 5,459,872 (Ex. 8), 16:29-35 ("In FIG. 8, the control software 264 is able to write directly into the interrupt register 261 thus enabling both the hardware interrupt requests from generators 260, . . . , 265 and software generated interrupts from control software 264 to be handled in a common, unified manner."); U.S. Patent No. 6,574,693 (Ex. 9) ("The preceding discussion has presented a method and apparatus for an efficient manner of handling interrupts within a computer system.").

46. Thus, there are at least five different types of interrupt requests discussed in the patent and cited art.

47. A person of skill in the art, having reviewed the intrinsic evidence, would appreciate that it refers to many different types of interrupts, including the five different types summarized above. Such a person would also understand that the '025 Patent claims refer to interrupts generally at some places, and "potential" interrupts specifically at other places. They would understand that potential interrupts are merely one type of interrupt, and that there are many other types of interrupts. They would not understand the general term "interrupt" in the claims to be narrowly restricted to only "potential" interrupts.

2. Priority level information or priority levels

48. I understand that Intel proposes restricting "priority level information" and "priority levels" such that those elements are "not rewritten by software when the system changes mode or context."

49. The elements at issue in claims 1, 9, and 17 do not restrict how priority level information or priority levels are "rewritten" when the system changes mode or context. A person of skill in the art would not interpret the claims by adding new requirements to them regarding such matters.

50. Further, the specification describes multiple ways this can be achieved, including either with software, or without software. In one example, the specification provides: "By implementing the interrupt priority register 212 as a read/write register, the assigned priority values may be updated or changed under software control." Ex. 5, 6:60-63. Another section of the patent similarly provides: "The context switch could be based on an OS [*i.e.*, Operating System] context ID, power management modes, security modes, and other system defined modes where priority levels would differ." *Id.*, Abstract. In still another example, the specification states: "By eliminating the requirement for software to manage the priority level changes before a context switch, interrupt processing can proceed with reduced latency and lower power consumption." *Id.*, 3:19-22. Potentially, any of these modes may be controlled by software, causing the interrupt priority register to be rewritten.

51. Accordingly, a person of ordinary skill in the art would understand that the inventors contemplated multiple possible approaches to changing priority level information or priority levels: some with software and some without software. A person of ordinary skill, particularly in the context of that disclosure, would not add limitations to the claims that restricted

the claims to just one or the other approach. To the contrary, a person of ordinary skill in the art would recognize that the patent described both approaches and included claims that encompassed both.

3. Definiteness

52. I have been informed by counsel that a patent must end with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as the invention. I understand that patent claims, read in light of the specification and prosecution history, must inform with reasonable certainty those skilled in the art about the scope of the invention. I understand that if a defendant shows by clear and convincing evidence that this requirement has not been met, the affected claims may be found invalid. I further understand that definiteness is evaluated from the perspective of one of ordinary skill in the art at the time of the invention. I have followed these principles here.

53. I understand that Intel argues that the following limitations in claim 1 are indefinite:

[(1)] providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode, and a second interrupt priority storage device for storing priority level information associated with a second system mode; and

[(2)] providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode **for each of the one or more interrupt requests**, and a second interrupt priority storage device for storing priority level information associated with a second system mode **for each of the one or more interrupt requests**;

54. These elements are the same except for the bolded language above.

55. I further understand that Intel argues:

A person of ordinary skill in the art would not understand whether the "a plurality of interrupt priority storage devices," "a first

interrupt priority storage device," "a first system mode," "a second interrupt priority storage device," and "a second system mode" recited in (1) is the same as the "a plurality of interrupt priority storage devices," "a first interrupt priority storage device," "a first system mode," "a second interrupt priority storage device," and "a second system mode" recited in (2).

Defendant Intel Corporation's Preliminary Invalidity Contentions (Ex. 10), 796-97.

56. A person of ordinary skill in the art would understand that the common portions of the two elements quoted by Intel could be satisfied by the same structures. Nothing in the claims suggests that different structures are required.

57. Indeed, a person of skill reviewing these claim terms would observe that where such differences were sought to be required, those differences were called for explicitly. For example, the terms require "a first system mode" and "a second system mode," as opposed to referring twice to "a system mode." Similarly, the terms require "a first interrupt priority storage device" and "a second interrupt priority storage device," as opposed to referring twice to "an interrupt priority storage device." A person of skill would understand, in this context, that if the inventors had wanted to require a first plurality of storage devices and a second, separate and distinct plurality of storage devices, they would have followed the same convention and said so. They did not, and there is no such requirement in these claim elements.

58. My review of the specification supports this conclusion. Nothing in the specification imposes a requirement of two different structures for elements (1) and (2).

59. I note further that there are material differences between the two elements. The second element, for instance, in two locations requires "for each of the one or more interrupt requests." Therefore, a person of skill would understand that any structure meeting the requirements of the second element must fit that full description, which is not a requirement of the

prior element. Because of this difference, a person of skill would appreciate that the two elements are not redundant.

Executed on this 30th day of October, 2019, in Marshall, TX.

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct to the best of my knowledge.

A handwritten signature in black ink, appearing to read 'T M Conte', with a long horizontal stroke extending to the right.

Thomas M. Conte, Ph.D.